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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/540,973	06/27/2005	Akira Tanabe	8013-1243	9220

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EXAMINER	
PARIHAR, SUCHIN	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/540,973	TANABE, AKIRA	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-26* is/are allowed.

6)☒ Claim(s) *1-4,6,8,9 and 11* is/are rejected.

7)☒ Claim(s) *5, 7,10 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/27/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 6 is objected to for the following reason: the following phrase lacks antecedent basis in the claims: "**wherein a measurement of the mutual conductance** is conducted under a bias condition". Claim 1, from which claim 6 depends, does not provide antecedence for a "measurement" of the mutual conductance, only a "calculation", wherein the two terms do not have the same meaning in the art. Examiner suggests applicant amend said language to clarify the claim.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claim 3, 4, 9 and 11 are rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 3, the following language is indefinite: "calculating a drain current **at around** a frequency of the AC input signal". The scope of "at around" cannot be reasonably determined or understood by one of ordinary skill in the art. Examiner suggests amending said language to clarify the claim language.

With respect to claims 4 and 9, the following language is found indefinite "**the AC input signal being inputted from a ratio** of a mutual conductance of the SOI MOSFET at a frequency of the AC input signal". The disclosure fails to clarify how a ratio, which is a number or quantitative measure, can be used to input the AC input signal, wherein

the AC input signal is a physical element, i.e. a electrical signal. Therefore, the claim is missing the functional relationship between "AC input signal" and "ratio", i.e. how can a ratio be used to input an AC input signal? Examiner suggests that the language be amended to clarify the claim's intended meaning.

With respect to claim 11, the following language is found indefinite, "that an absolute value of the gate voltage is **within 0.5 V**". With respect to "within 0.5 V", there is no specified range or comparison. Examiner suggests Applicant see claim 6 as an example, i.e. within 0.5 V of what quantity or measure?

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-2, 6 and 8 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Tamegaya (US 6,295,630) in view of Sugano et al. (US 6,734,501).

6. With respect to claims 1 and 8, Tamegaya teaches:

an AC input signal (see Figure 1, #3, input unit) superimposing circuit (see Figure 1, #3, input unit) for superimposing an AC input signal (see Figure 3, 222, AC input) to a gate/drain (gate and drain, Col 3, lines 5-20) of a MOSFET (MOSFET, Col 1, lines 10-20);

an AC component measurement circuit (see Figure 1, measuring portion 22) for measuring an AC component of a current flowing (measuring electric current flowing,

Col 11, lines 20-35) between a source and a drain (source/drain, Col 11, lines 20-35) of the MOSFET (MOSFET, Col 1, lines 10-20) when the AC input signal is superimposed to the gate/drain (gate and drain, Col 3, lines 5-20); and

wherein the gate, source and drain (source, drain and gate, Col 11, lines 20-35) of the MOSFET are being applied a DC voltage (see capacitor of Figures 4 and 8 supplying DC voltage).

Tamegaya fails to teach:

A mutual/drain conductance calculation circuit for calculating a mutual conductance at a frequency of the AC input signal of the MOSFET from a ratio of amplitude of an AC component of a measured current and amplitude of the AC input signal.

However, Sugano teaches:

a mutual/drain conductance calculation (mutual conductance calculation, see Col 3, lines 8-20) circuit for calculating a mutual conductance at a frequency of the AC input signal of the MOSFET (MOSFET, Col 1, lines 10-20) from a ratio of amplitude of an AC component of a measured current (source/drain current, Col 3, lines 1-40) and amplitude of the AC input (input voltage, Col 3, lines 1-40) signal (mutual conductance calculation, see Col 3, lines 8-20).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Sugano in the invention of Tamegaya for at least the following reason:

Sugano improves the invention of Tamegaya by providing a method wherein the mutual conductance can be calculated and increased which is a desirable attribute in the art (see Sugano, Col 2,lines 60-68).

7. With respect to claim 2, Tomegaya in view of Sugano teaches:

wherein the MOSFET is a SOI MOSFET having a SOI structure (see Sugano, title, SOI MOSFET).

8. With respect to claim 6, Tomegaya teaches:

wherein a measurement of the mutual conductance is conducted under a bias condition (bias voltage, Col 5, lines 40-45) that the gate voltage is within 0.5 V of a threshold value (threshold voltage, Col 2, lines 5-10) of the MOSFET.

Allowable Subject Matter

9. Claims 5, 7, 10 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claims 5 and 10, the prior art of record fails to teach:

a comparator circuit for comparing a gate .cndot. source .cndot. drain voltage dependency of a frequency characteristic of the mutual conductance obtained from the mutual conductance calculation circuit as a result of measurement of the MOSFET with a gate .cndot. source .cndot. drain voltage dependency of a frequency characteristic of the mutual conductance obtained as a result of circuit simulation for simulating the MOSFET.

With respect to claims 7 and 12, the prior art of record fails to teach:

wherein the AC input signal superimposing circuit superimposes the AC input signal to the gate under a condition of applying the DC voltage to the substrate as well as the gate, the source, and the drain.

10. Claims 13-26 allowed for the following reason:

With respect to claims 13, 17, 20 and 24, the prior art of record fails to teach:

a step for comparing a gate .cndot. source .cndot. drain voltage dependency of a frequency characteristic of the mutual conductance obtained as a result of measurement of the MOSFET with a gate .cndot. source .cndot. drain voltage dependency of a frequency characteristic of the mutual conductance obtained from circuit simulation for simulating the MOSFET; and

a step for changing a parameter which is used for the circuit simulation so that a frequency characteristic of the mutual conductance obtained as a result of the circuit simulation approaches to a frequency characteristic of the mutual conductance obtained from a result of measurement of the MOSFET, wherein the gate, the source, and the drain of the MOSFET are being applied a DC voltage.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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PRIMARY EXAMINER